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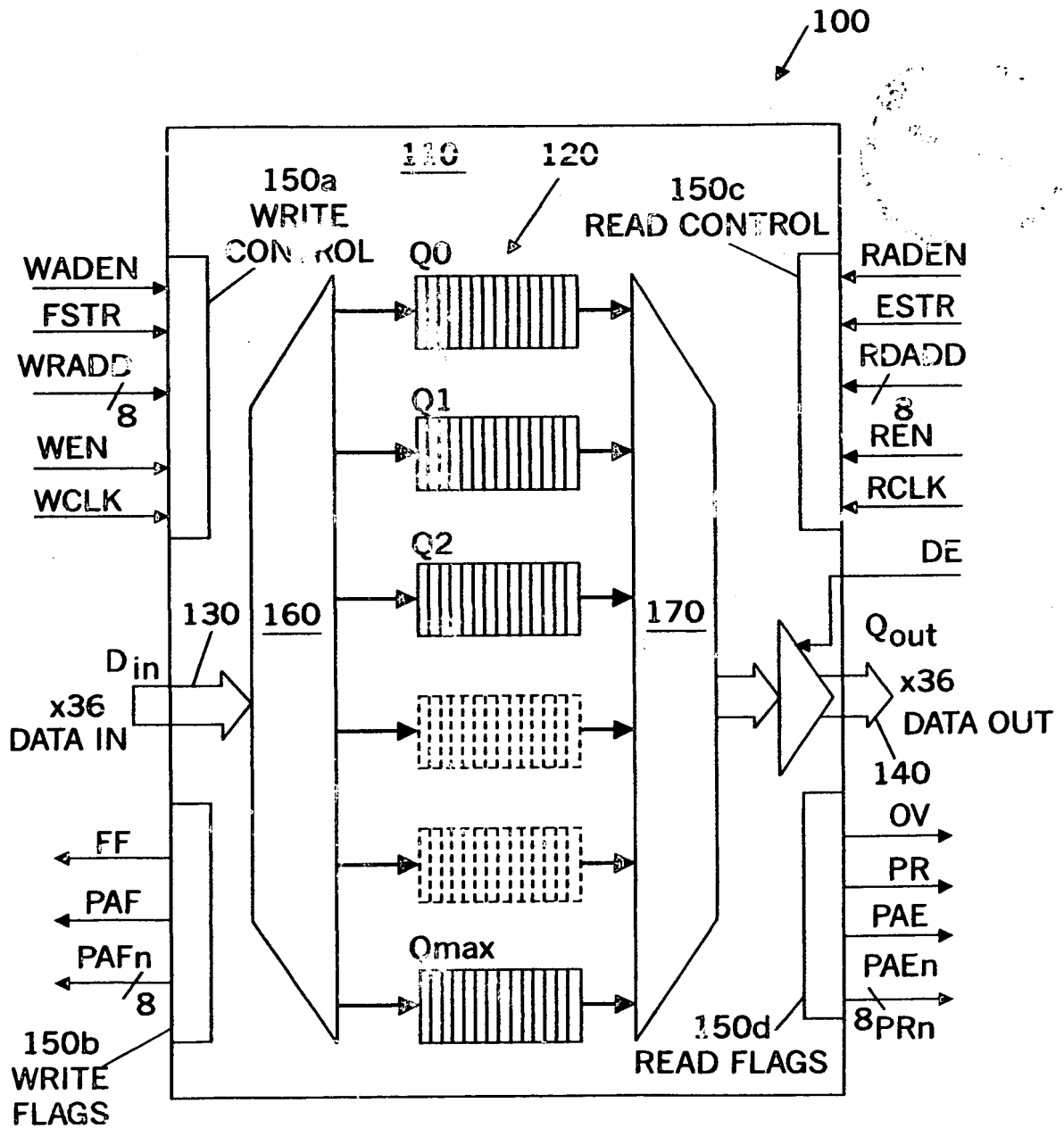
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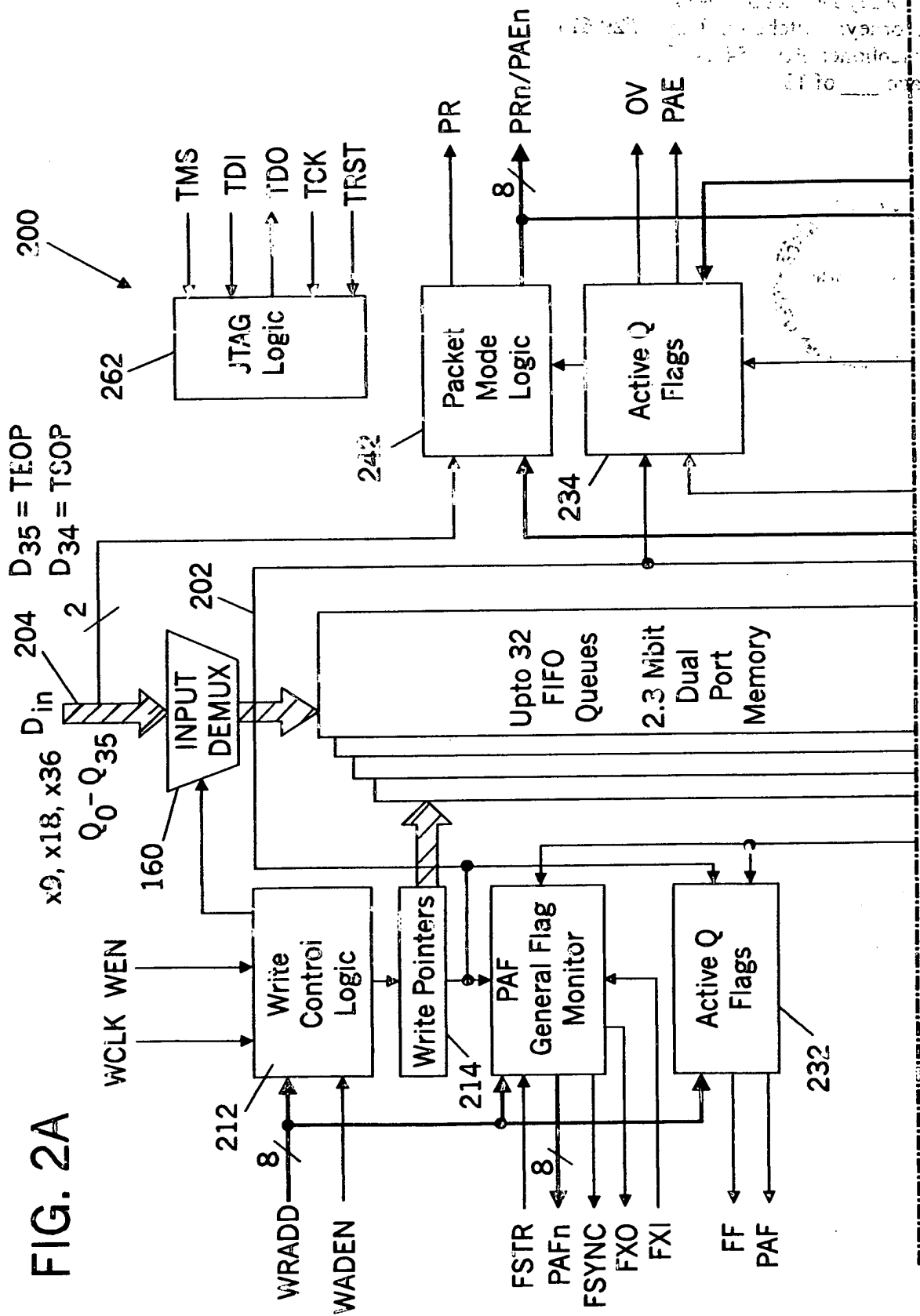
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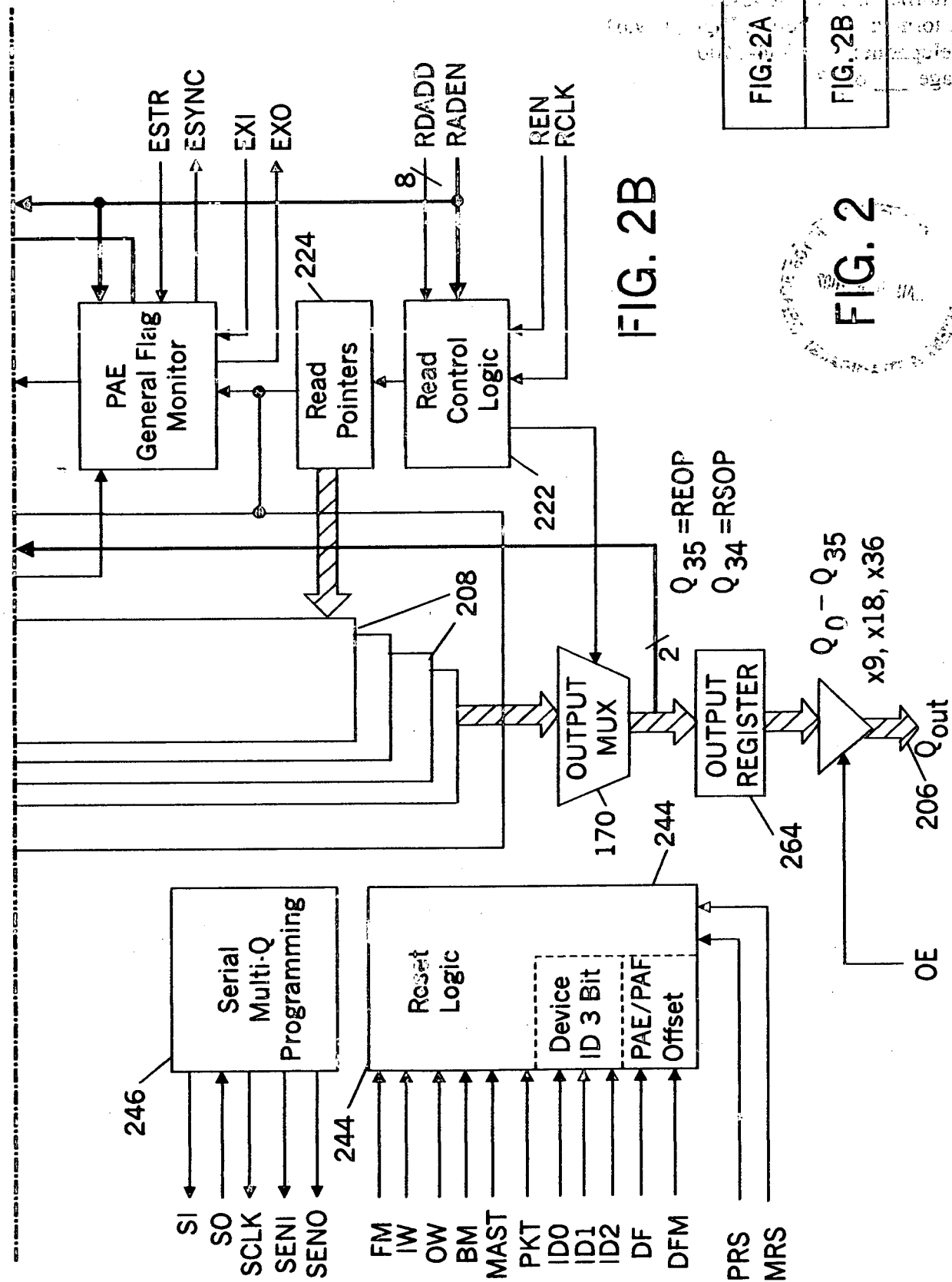
FIG. 1



**FIG. 2A**

FIG. 2A is a block diagram of a memory controller system. The system includes an INPUT DEMUX (202) which receives data from a source (204) via D<sub>in</sub> (x9, x18, x36) and Q<sub>0</sub>-Q<sub>35</sub>. The demux outputs to a Write Control Logic (212) and a Write Pointers block (214). The Write Control Logic (212) also receives WCLK and WEN signals and outputs WRADD (8-bit) and WADEN to the Write Pointers block. The Write Pointers block (214) outputs to a PAF General Flag Monitor (232) and an Active Q Flags block (234). The PAF General Flag Monitor (232) outputs FSTR, PAF<sub>n</sub> (8-bit), FSYNC, FXO, and FXI signals. The Active Q Flags block (234) outputs FF and PAF signals. The system also includes a Packet Mode Logic block (242) and an Active Q Flags block (234). The Packet Mode Logic block (242) receives PR and PR<sub>n</sub>/PAE<sub>n</sub> (8-bit) signals and outputs to the Active Q Flags block (234). The Active Q Flags block (234) outputs OV and PAE signals. The system also includes a JTAG Logic block (262) with TMS, TDI, TDO, TCK, and TRST signals. The system also includes a memory block (204) with D<sub>35</sub> = TEOP and D<sub>34</sub> = TSOP signals.





2B

**FIG. 2A**

Fig. 2B

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FIG. 3

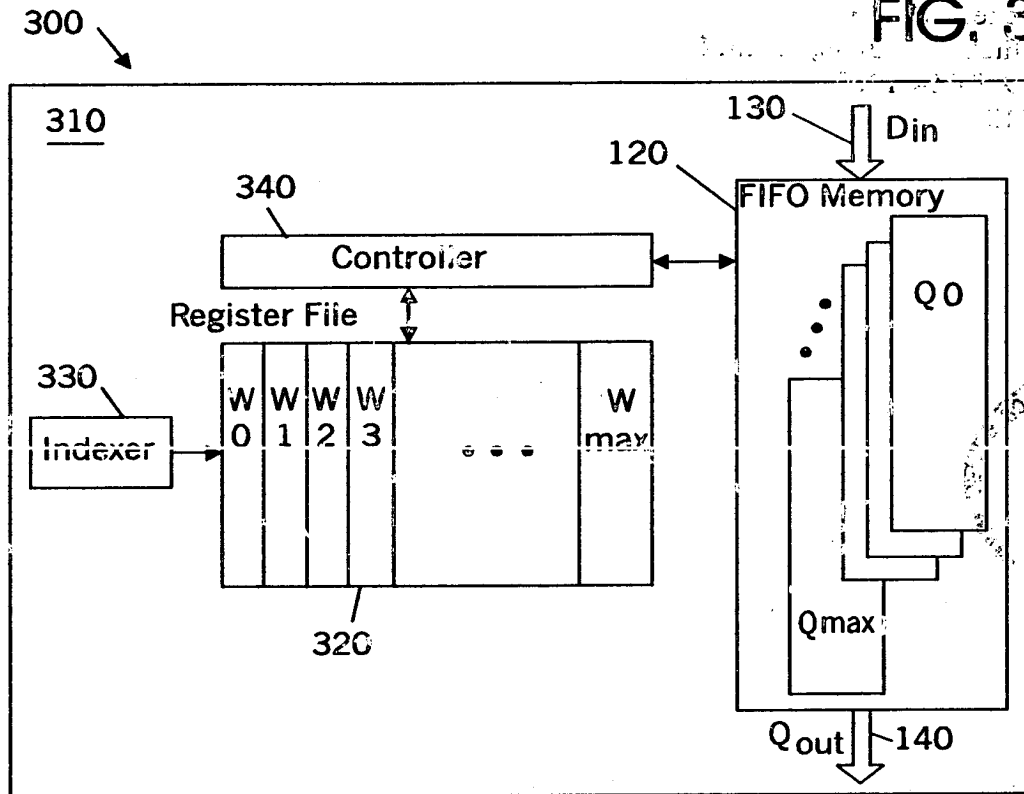


FIG. 4

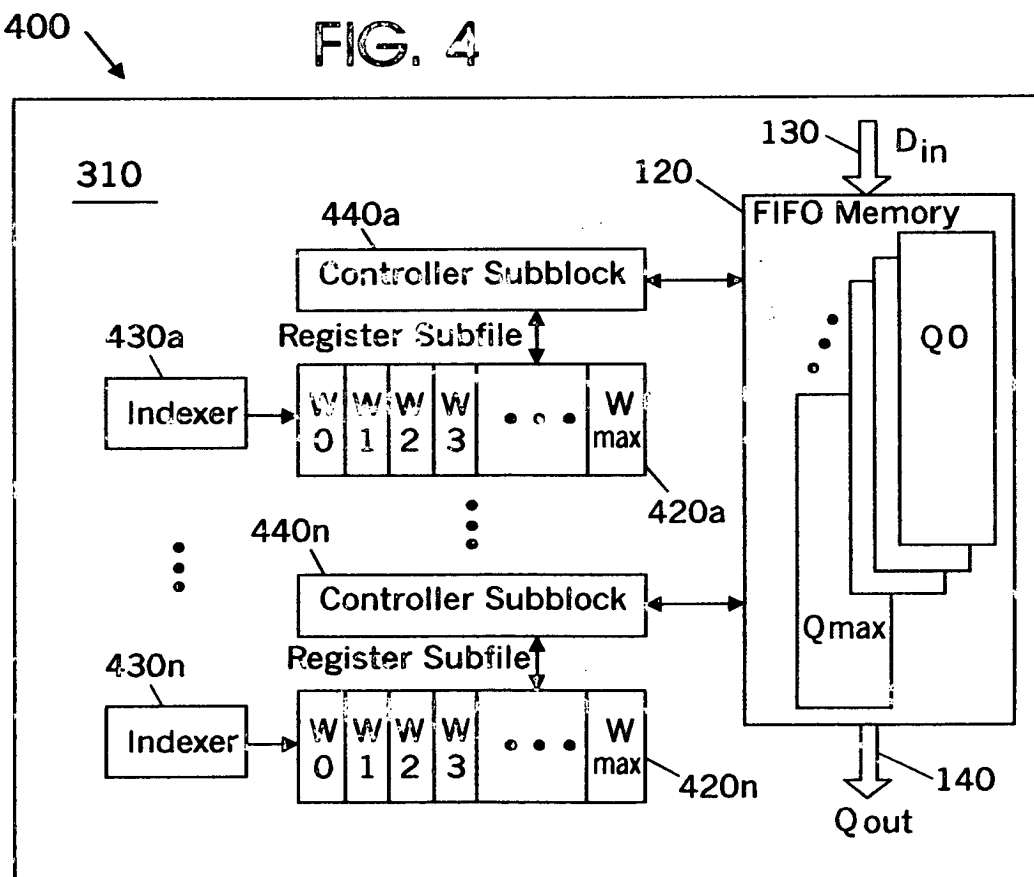
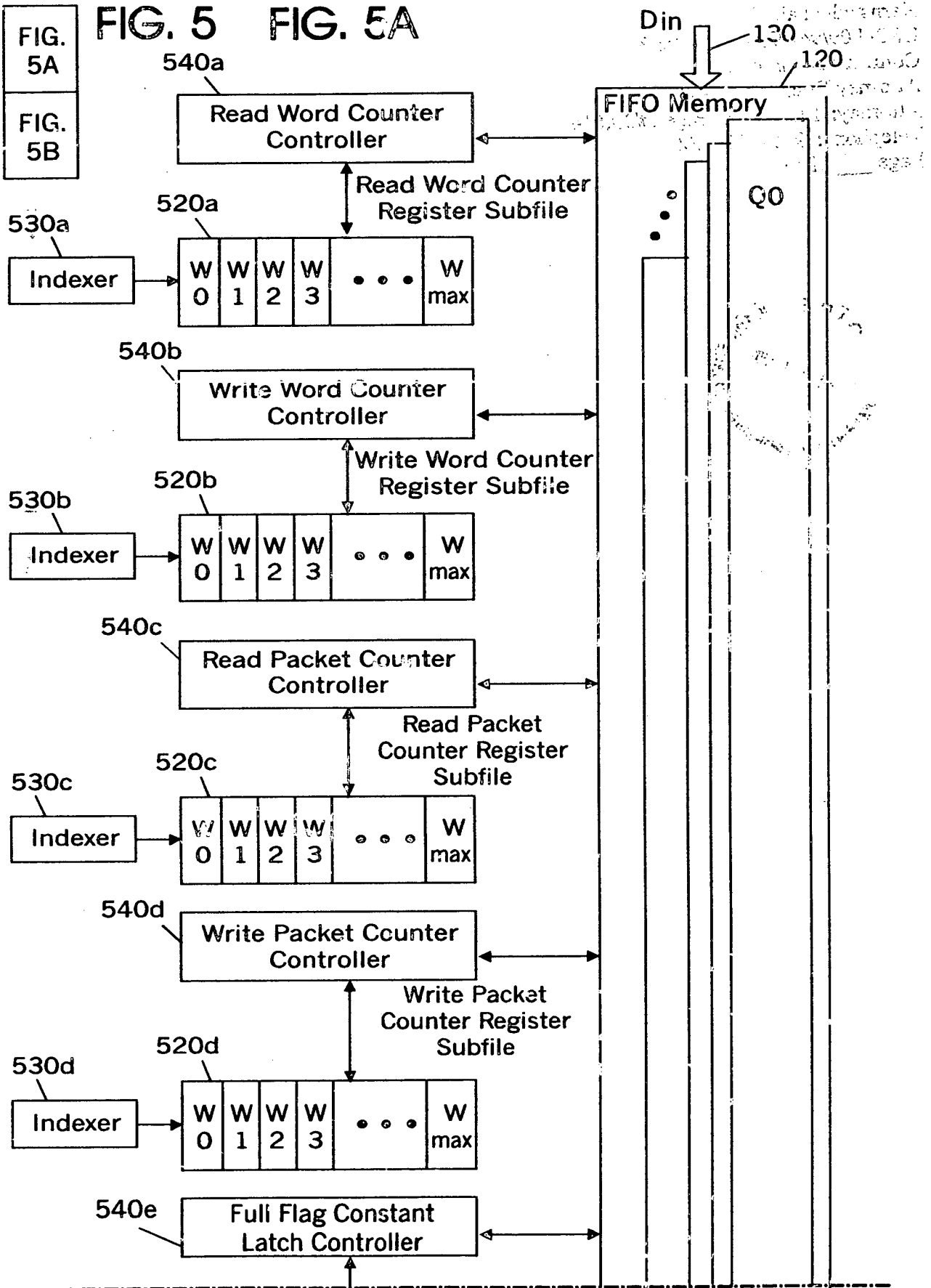


FIG. 5A  
FIG. 5B

FIG. 5 FIG. 5A



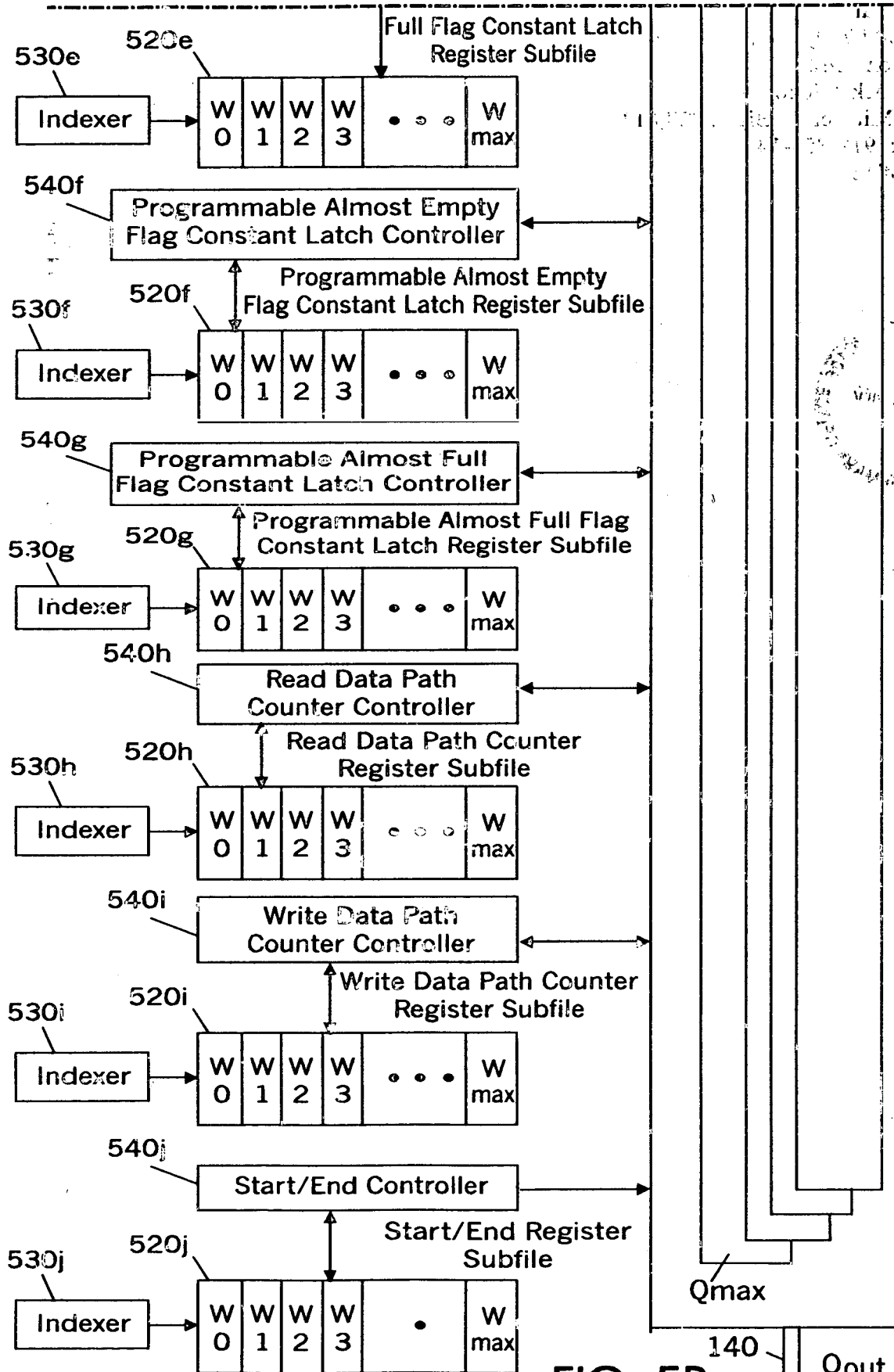


FIG. 5B

FIG. 6

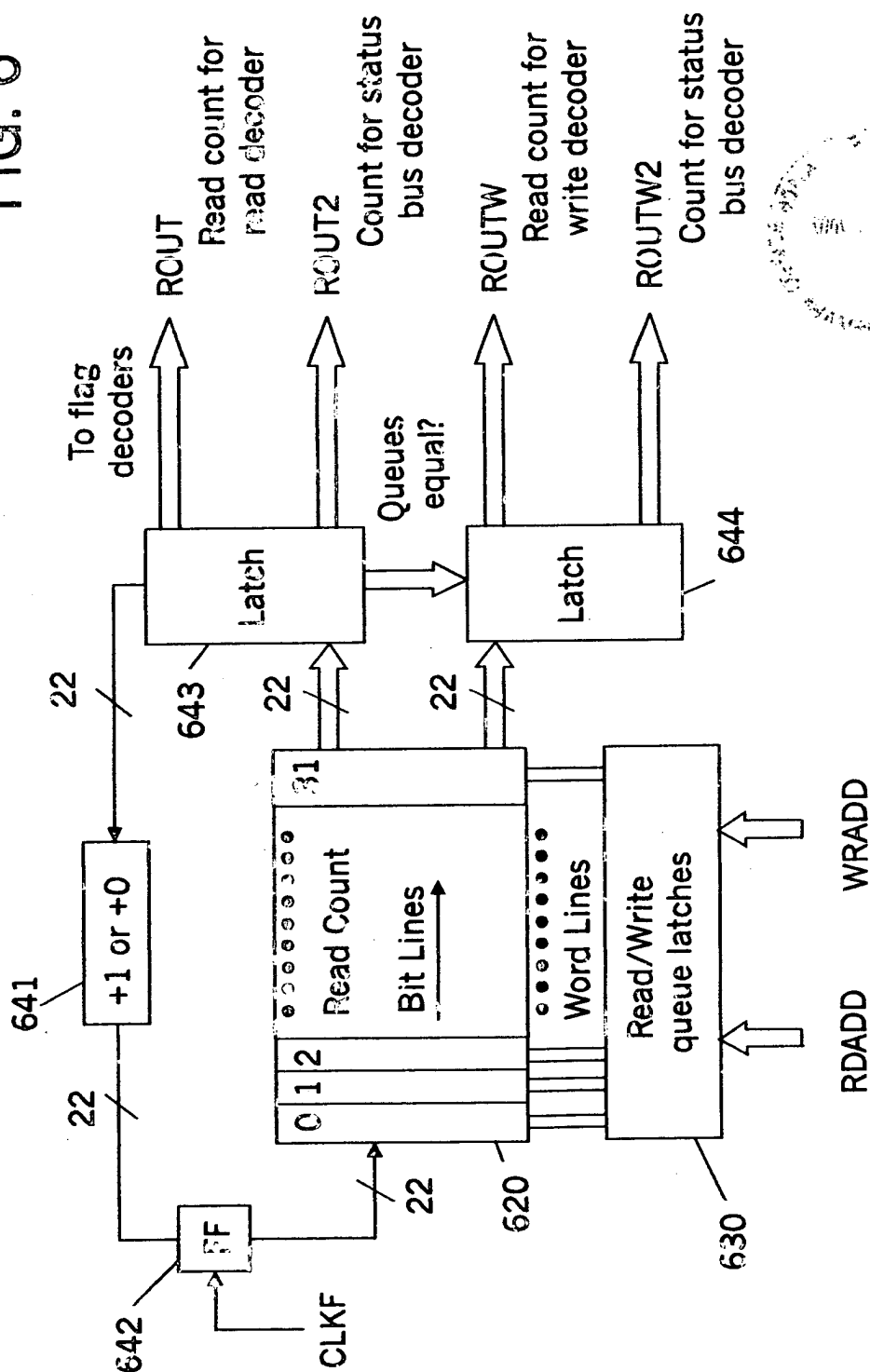




FIG. 7

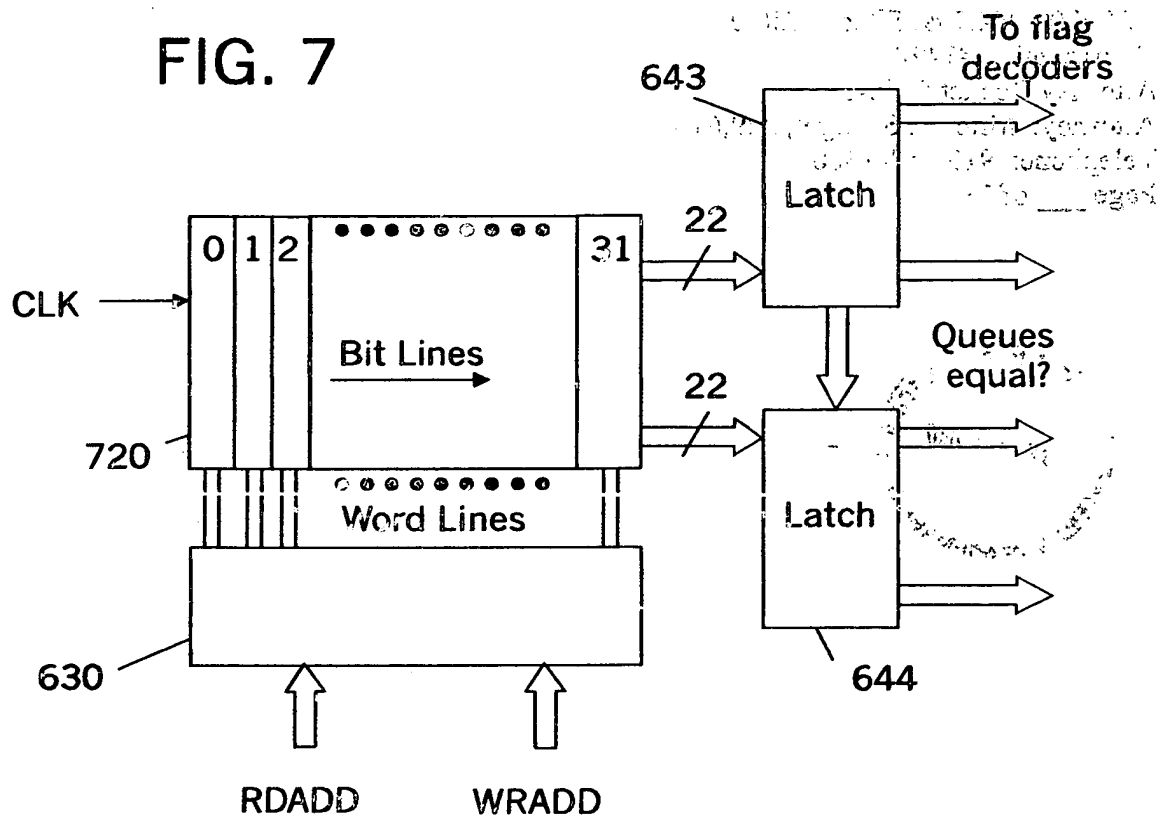


FIG. 14

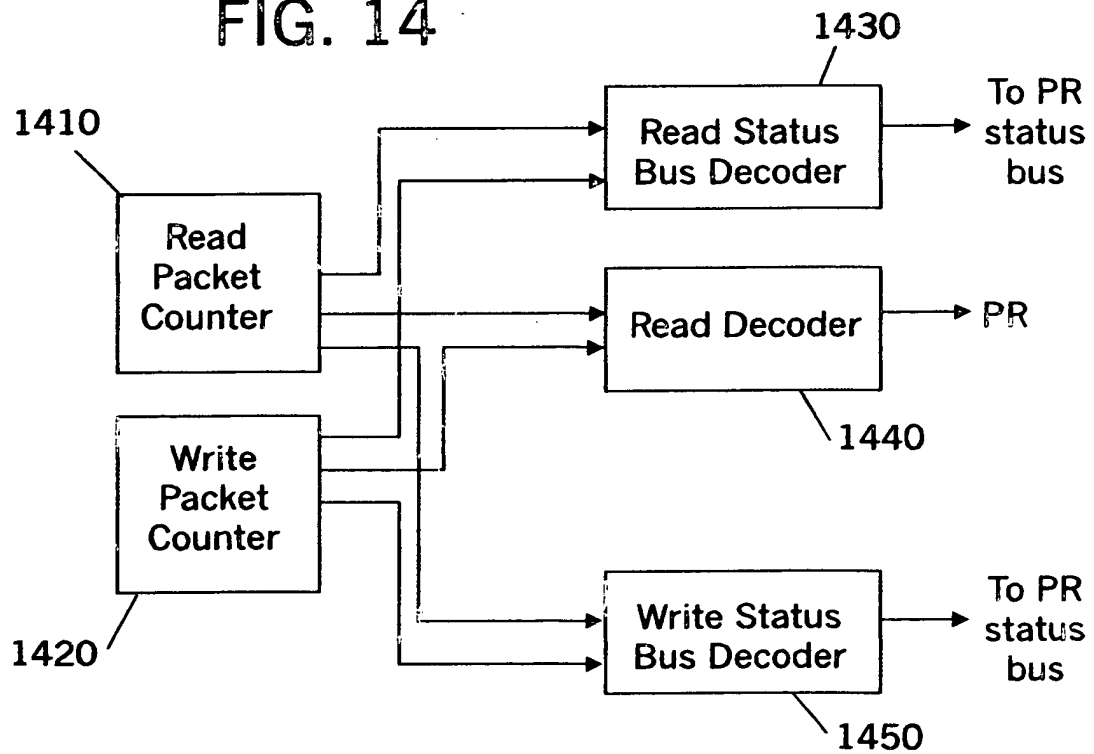


FIG. 8

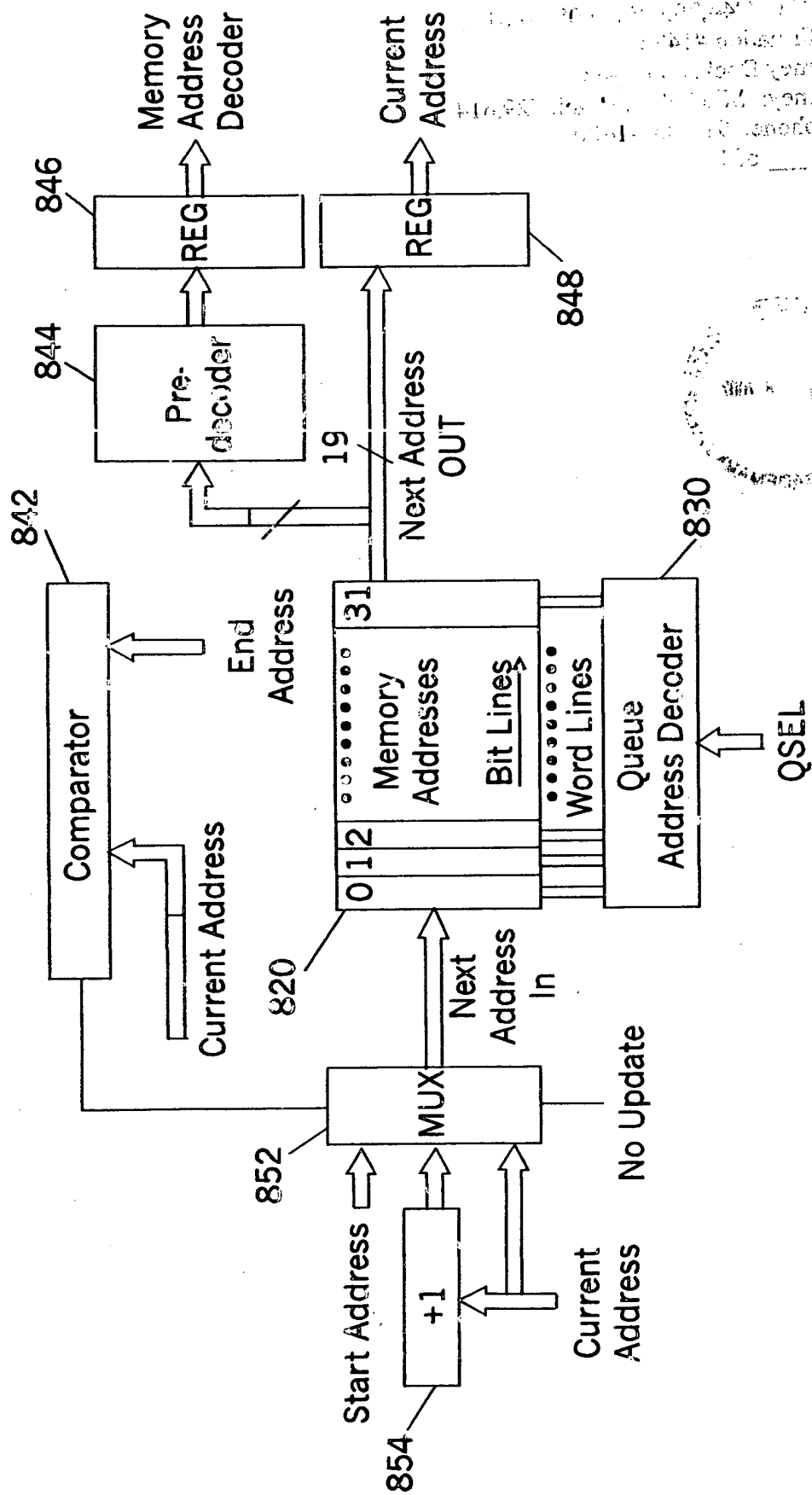


FIG. 9

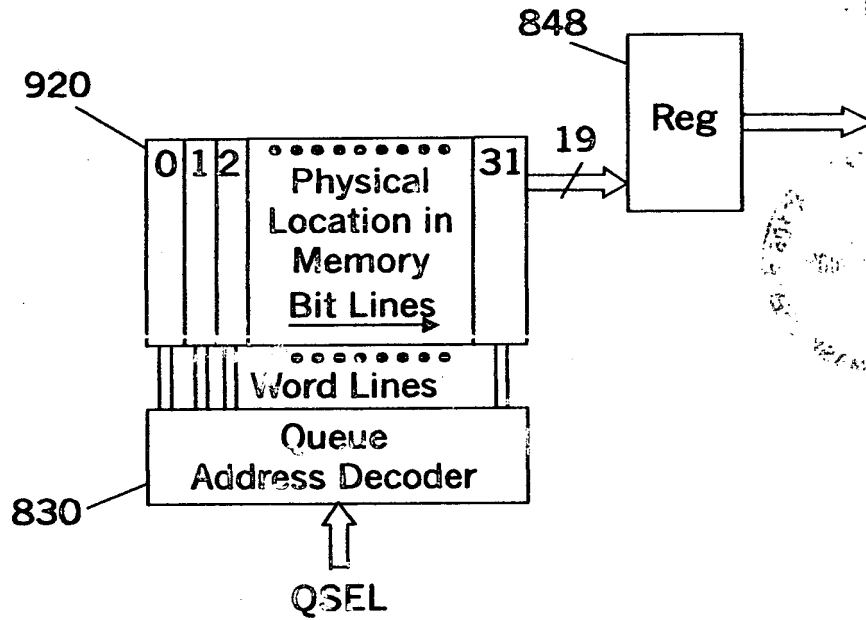


FIG. 13

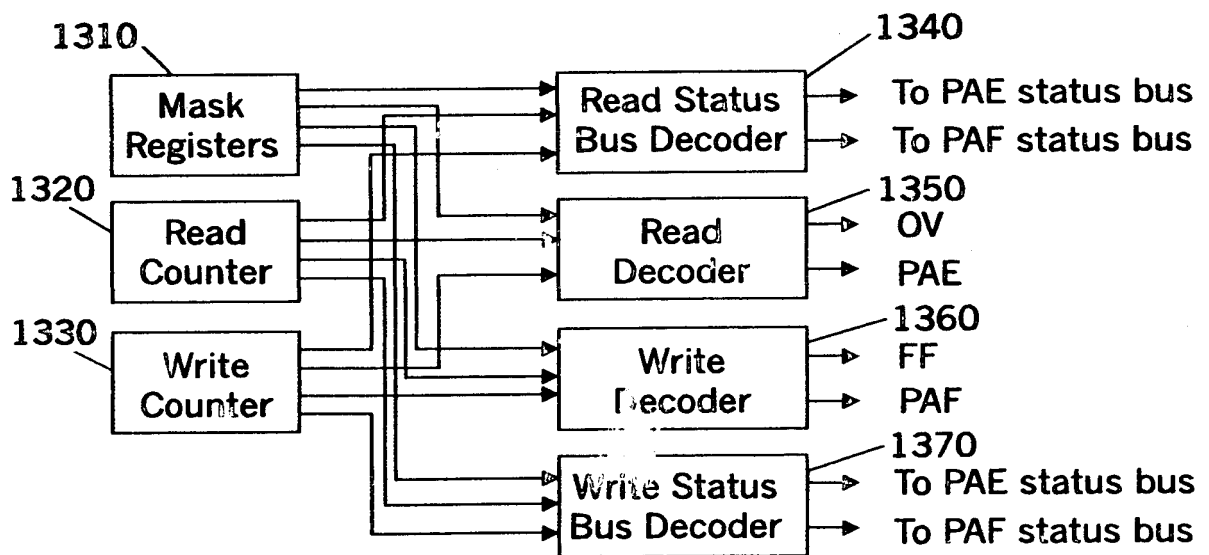


FIG. 10

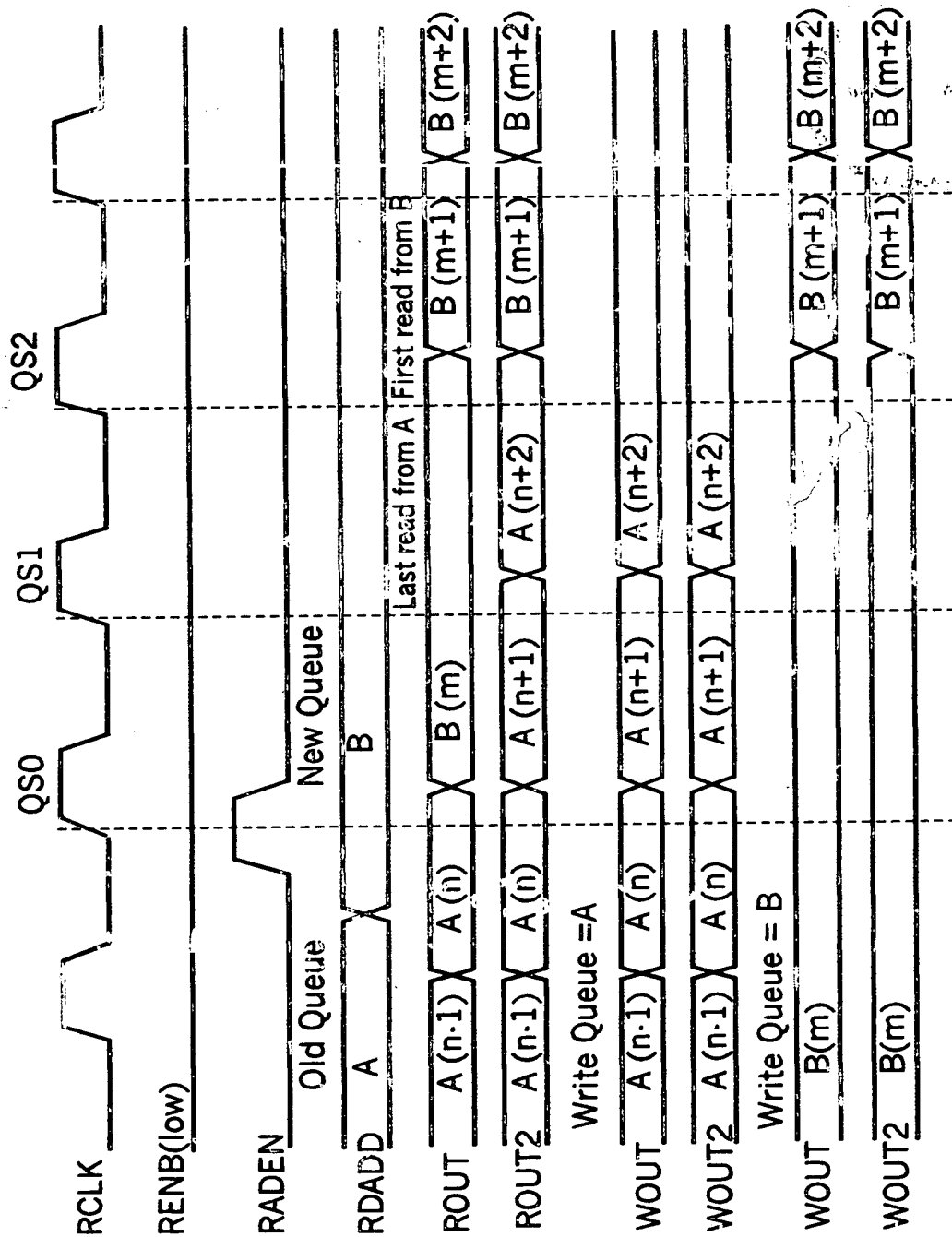


FIG. 11

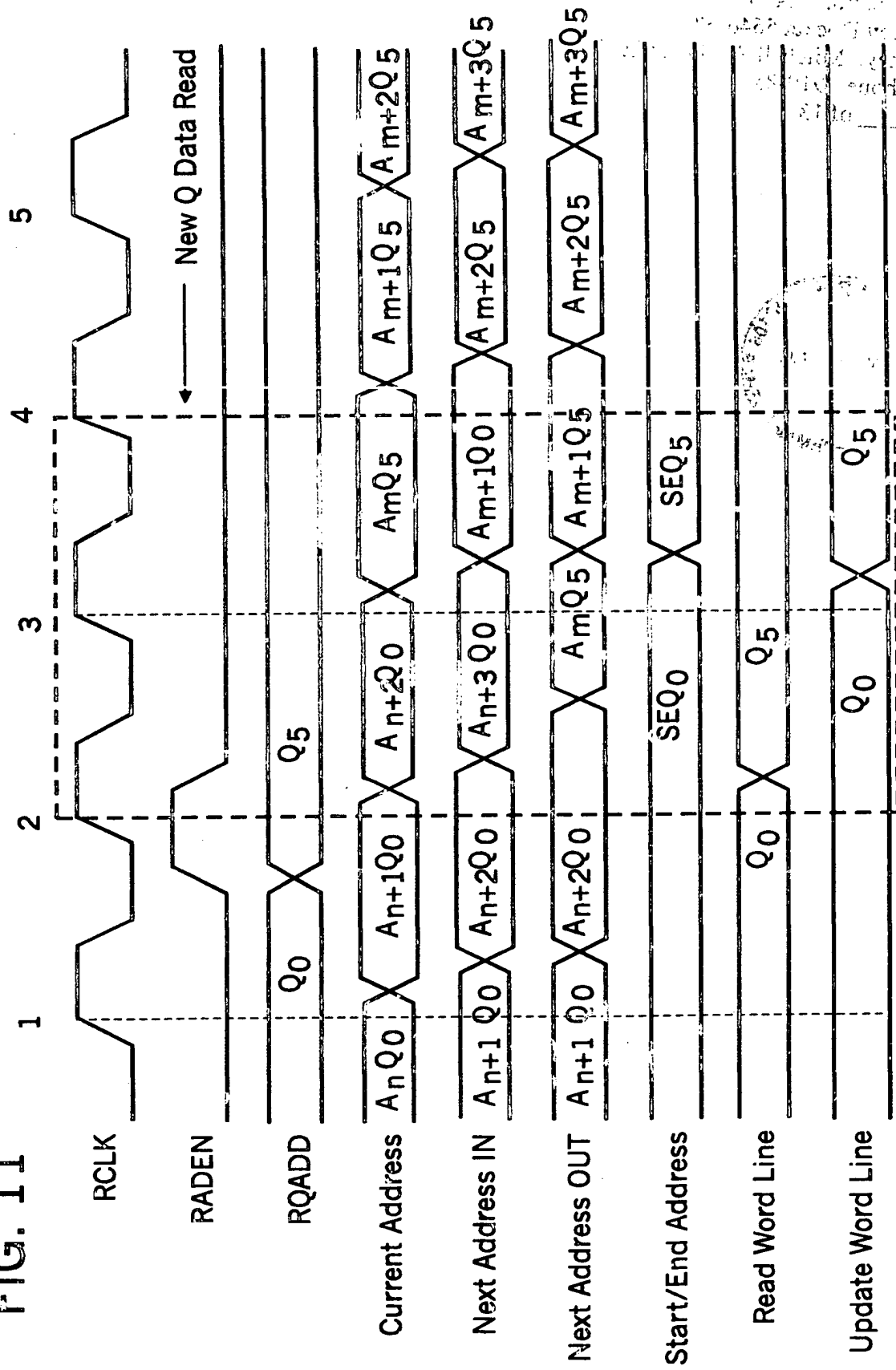


FIG. 12

